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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-16 (cancelled)

17. (currently amended) A nonvolatile memory device comprising:

a control circuit;

a data terminal;

a plurality of latch circuits;

a plurality of nonvolatile memory cells;

a plurality of word lines; and

a first decode circuit,

wherein each of said memory cells couples to a corresponding word line, couples to a corresponding latch circuit, and is capable of having a threshold voltage within one of a plurality of threshold voltage ranges,

wherein said first decode circuit decodes data, receives data having a plurality bits from said data terminal, and outputs a first signal to said plurality latch ~~circuit~~circuits, said first signal having two states,

and

wherein in a program operation, said control circuit controls ~~to~~ receiving of data, ~~to~~ decoding of data by said first decode circuit, ~~to~~ latching of said first signal in a first state at a first said latch circuit coupled to a first memory cell ~~objected~~ to be subjected to a first level programming, ~~to~~ supplying a program voltage to a word line coupled to said first memory cell after latching at said first latch circuit, ~~to~~ latching of said first signal in said first state at a second said latch circuit coupled to a second memory cell ~~objected~~ to be subjected to a second level programming, and ~~to~~ supplying said program voltage to a word line coupled to said second memory cell after latching at said second latch circuit.

18. (currently amended) A nonvolatile memory device according to claim 17, further comprising a buffer circuit,

wherein ~~said~~ a buffer circuit couples between said data terminal and said first decoder circuit for buffering data from said data terminal.

19. (currently amended) A nonvolatile memory device according to claim 18, further comprising a plurality of data lines,

wherein each of said data lines couples to a corresponding memory cell and couples to a corresponding latch circuit, and

wherein in said program operation, said each latch circuit supplies a second signal to ~~said~~ the corresponding memory cells during said supplying of program voltage via said data line when said latch circuit ~~is set~~ has latched said first signal.

20. (currently amended) A nonvolatile memory device according to claim 19,

wherein in said program operation, said control circuit controls ~~to~~ supplying of one voltage level of verify voltages to ~~said~~ a selected word line, ~~to~~ judging of a threshold voltage level of a memory cell which is supplied with said second signal, and ~~to~~ supplying of said program voltage to said selected word line and supplying said second voltage to a memory cell of which said threshold voltage ~~of which~~ level has not ~~been~~ reached a ~~preliminary voltage~~ level corresponding to a target programming level, and

wherein each of said verify voltages ~~is corresponding~~ corresponds to one of said plurality of threshold voltage ranges.

21. (currently amended) A nonvolatile memory device according to claim 20, further comprising a second decode circuit,

wherein said second decode circuit decodes an address ~~receiving~~ received from outside for ~~selecting~~ word line selection.

22. (currently amended) A nonvolatile memory device according to claim 21,

wherein one of said threshold voltage ranges ~~is indicated~~ indicates an erase state and others of said threshold voltage ranges ~~is indicated~~ indicates program states.

23. (currently amended) A nonvolatile memory device according to claim 22,

wherein in an erase operation, threshold voltages of memory cells coupled to said word line are ~~moved~~ shifted into the threshold voltage range ~~indicated~~ indicating said erase state.